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**EE 4550L**

**IC Hardware Security and Trust LAB**

**SPRING 2024**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 6th February 2024**

**Report due date: 8th February 2024**

1. **OBJECTIVE**

To practice schematic design in Cadence. To analyze, design, and use a trojan in Cadence.

1. **PROCEDURE**

Design a 1-bit adder, make the necessary basic gates in Cadence, make the 1-bit adder in Cadence, make a 4-bit adder subtractor in Cadence, and simulate them all in Cadence. Design a trojan in Cadence, simulate the trojan in Cadence, insert the trojan into the 4-bit adder subtractor in Cadence and simulate the 4-bit adder subtractor with the trojan.

1. **RESULT**

A computer screen shot of a computer circuit

Description automatically generated

Inverter schematic.

A screen shot of a graph

Description automatically generated

Exhaustive testing for inverter schematic above

A computer screen shot of a computer circuit

Description automatically generated

NAND2 schematic.

A screen shot of a computer screen

Description automatically generated

Exhaustive testing for NAND2 schematic above.

A computer screen shot of a circuit

Description automatically generated

NAND3 schematic.

A screenshot of a computer screen

Description automatically generated

Exhaustive testing for NAND3 schematic above.

A computer screen shot of a circuit board

Description automatically generated

XOR2 schematic.

A screen shot of a computer screen

Description automatically generated

Exhaustive testing for XOR2 schematic above.

A computer screen shot of a diagram

Description automatically generated

1-bit full adder schematic

A screen shot of a computer

Description automatically generated

Exhaustive testing for 1-bit full adder schematic above.

A computer screen shot of a diagram

Description automatically generated

4-bit full adder subtractor schematic.

A screen shot of a graph

Description automatically generated

Specific test cases for the 4-bit full adder subtractor above.

A screen shot of a graph

Description automatically generated

Delay for the 4-bit full adder subtractor above, only some rising delays are available based on the given test cases which result to an average rising delay of 293.789ps.

A diagram of a circuit

Description automatically generated

The critical path for the 4-bit full adder subtractor above.

A computer screen shot of a computer network

Description automatically generated

Trojan that I designed, it weakens the input signal, adds noise, and adds some delay. It is always on.

A screenshot of a computer screen

Description automatically generated

Waveform of the trojan I designed.

A computer screen shot of a diagram

Description automatically generated

4-bit adder subtractor schematic with the trojan added to it.

A screenshot of a computer screen

Description automatically generated

Waveform of the 4-bit adder subtractor with the trojan added in. As seen in the difference between Tro\_Sig\_In and Tro\_Sig\_Out, when the signal changes from a digital 1 to a digital 0, it slows down how quickly the signal changes and doesn’t let the signal reach a strong 1 or a strong 0. This causes the output to be incorrect as can be seen in COUT and S where during the time period where Tro\_Sig\_Out is “1?”, COUT is a 1 when it should be a 0 and S is 0101 where it should be 1101.

A graph with lines and text

Description automatically generated with medium confidence

This is the graph showing the delay of the 4-bit adder subtractor with the trojan. Only some delays are visible with the given test cases. With the given test cases, the average propagation delay is 290.2736ps.

The trojan weakening the signal can also be seen in the bottom two waveforms, where the voltage of the signal before and after the trojan can be compared. As can be seen in the before trojan signal, the difference in voltage between VDD and VSS is in the microvolt range. The difference after the trojan, however, is 169.3369 mV between VDD and the signal and 721.4475 mV between VSS and the signal.

1. **CONCLUSION**

My results satisfy the requirements, as I get correct outputs for all the given inputs for the 4-bit adder subtractor without the trojan and my trojan produces the expected results for what I designed it for. It is possible to improve my design to get better results because I did not put much effort into optimizing the gate sizes at a transistor level for the adder subtractor and it is likely that there is a way to design a trojan that can better do the functionality my trojan has by modifying the transistors in its design. I have learned how to design a basic trojan.